

**FIG. 1**

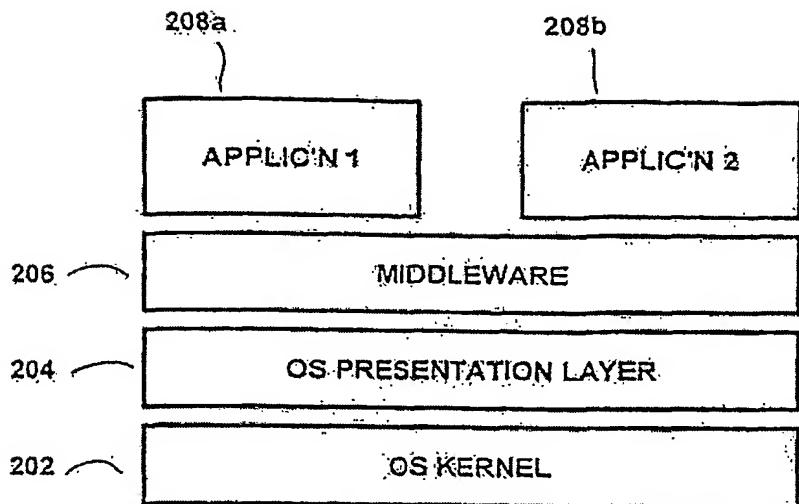


FIG. 2a

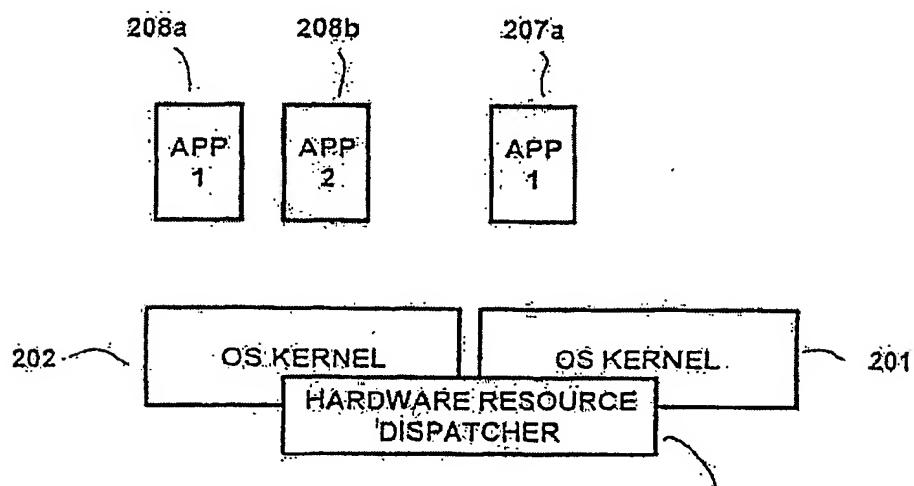
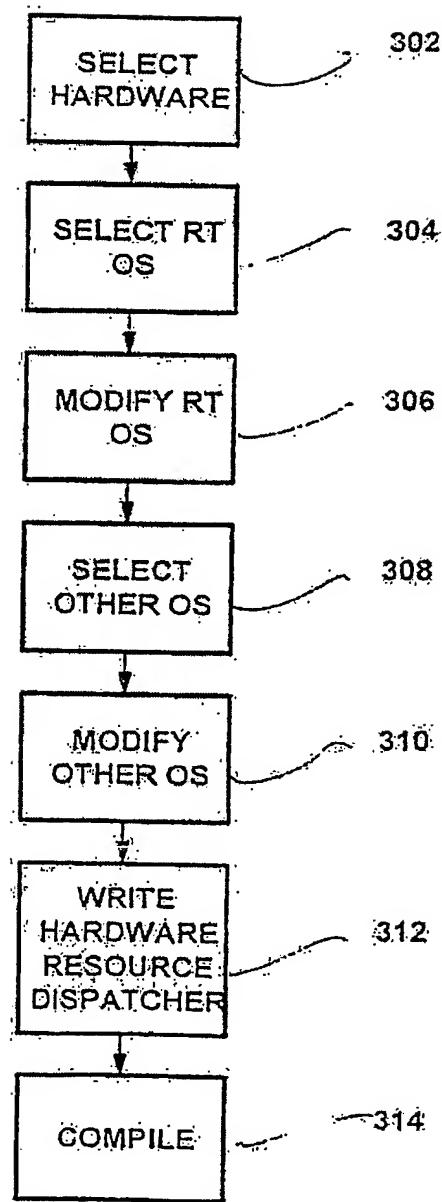
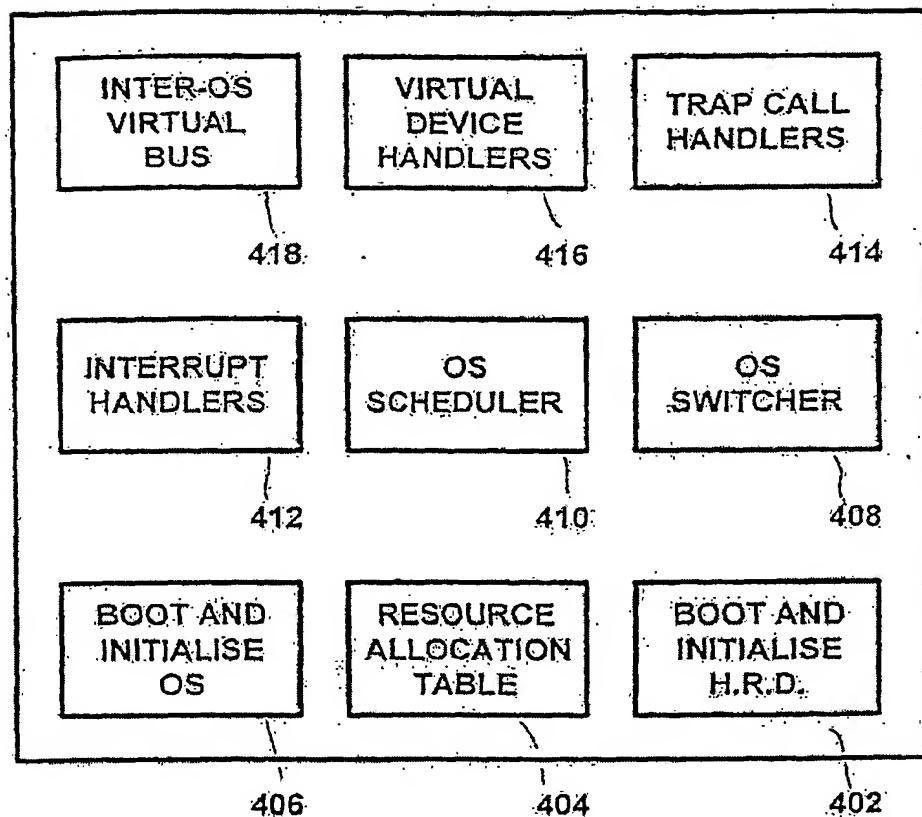


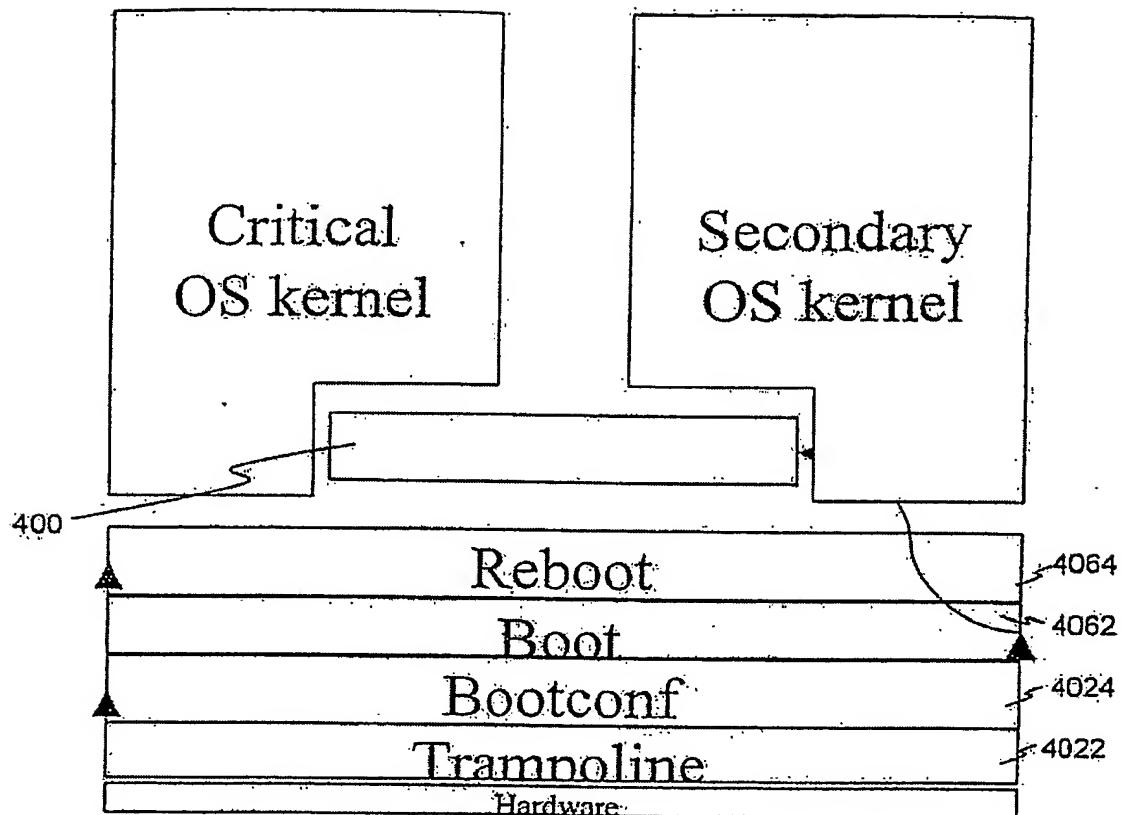
FIG. 2b

400

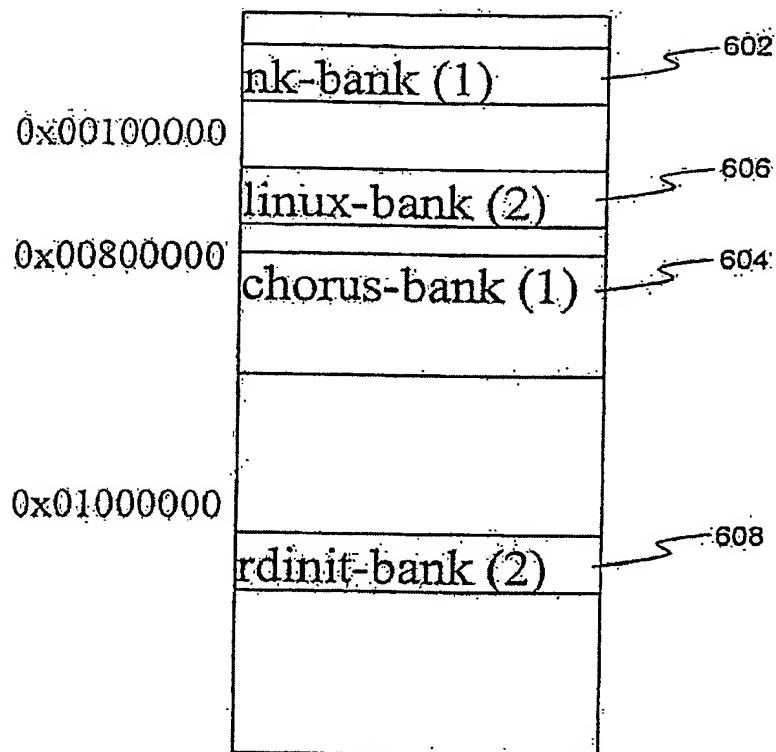
**FIG. 3**



**FIG. 4**



**FIG. 5**



**FIG. 6**

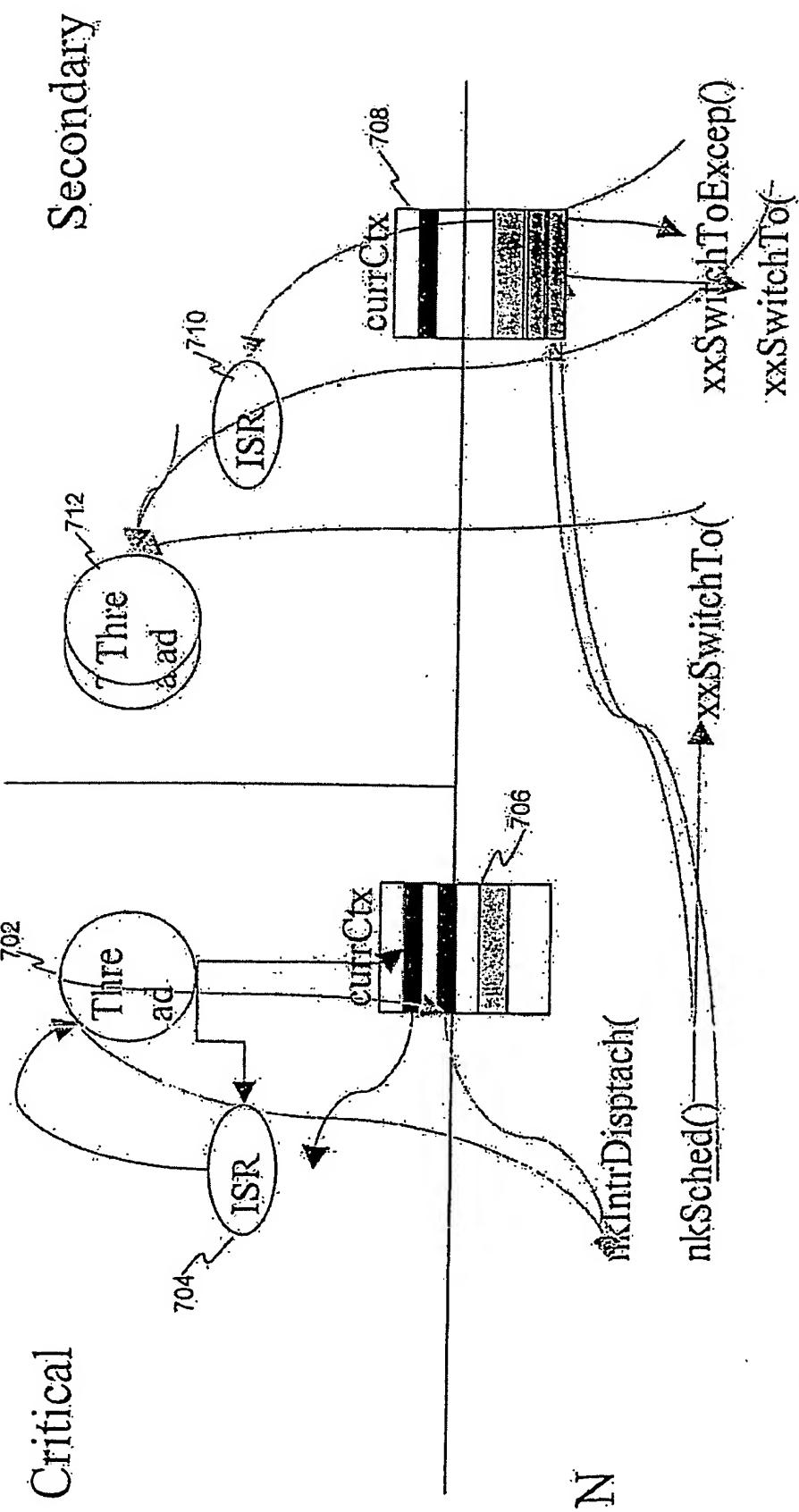


FIG. 7

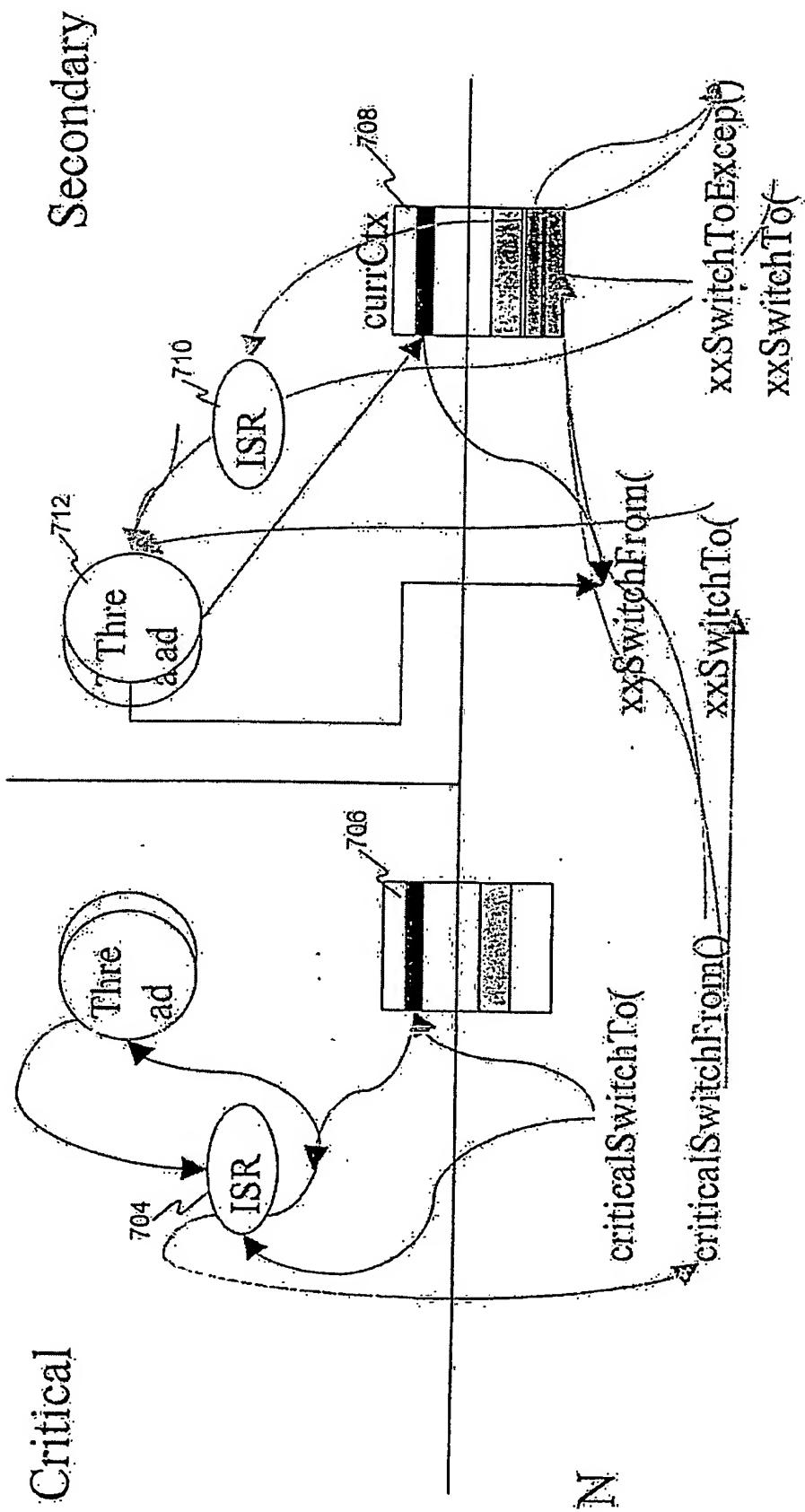
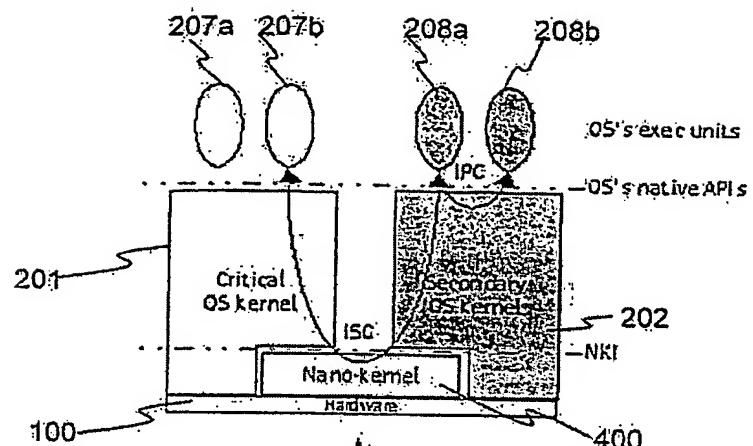
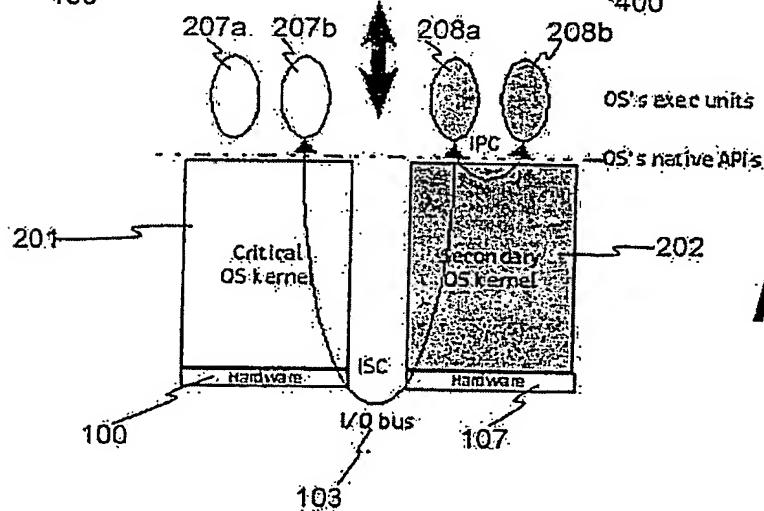


FIG.

**FIG. 9a****FIG. 9b**

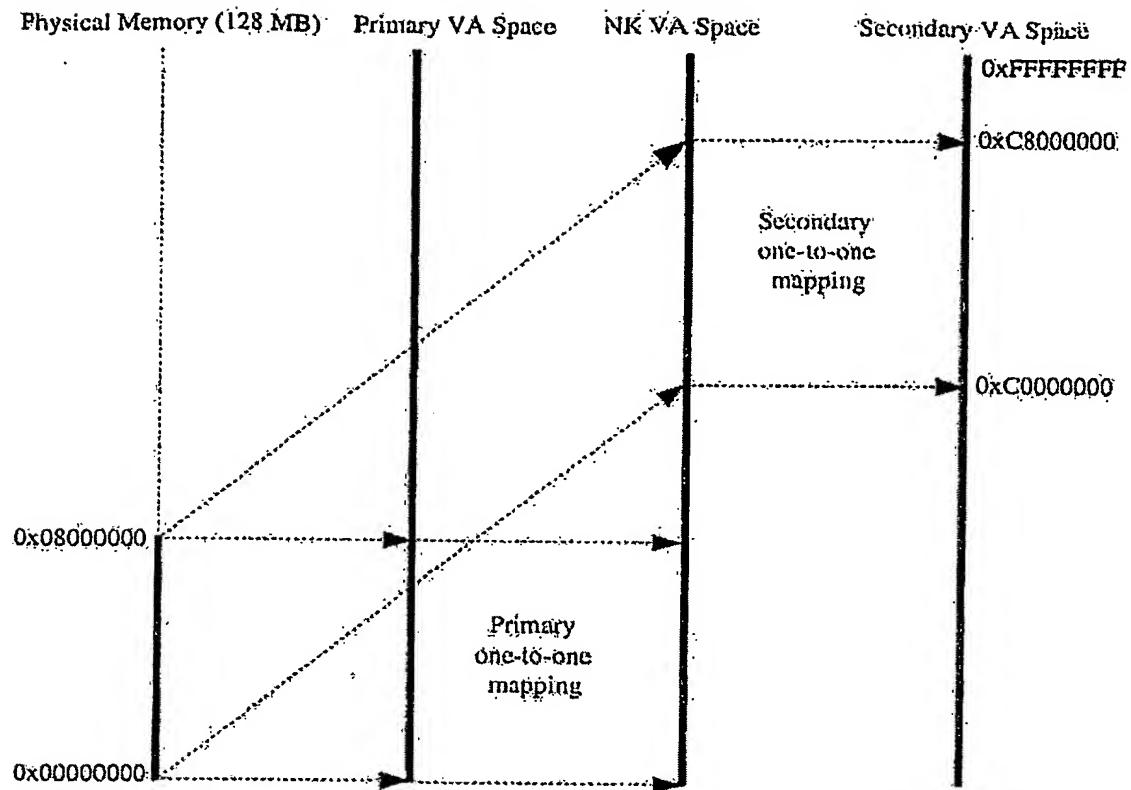


Fig. 10 Virtual Address Spaces

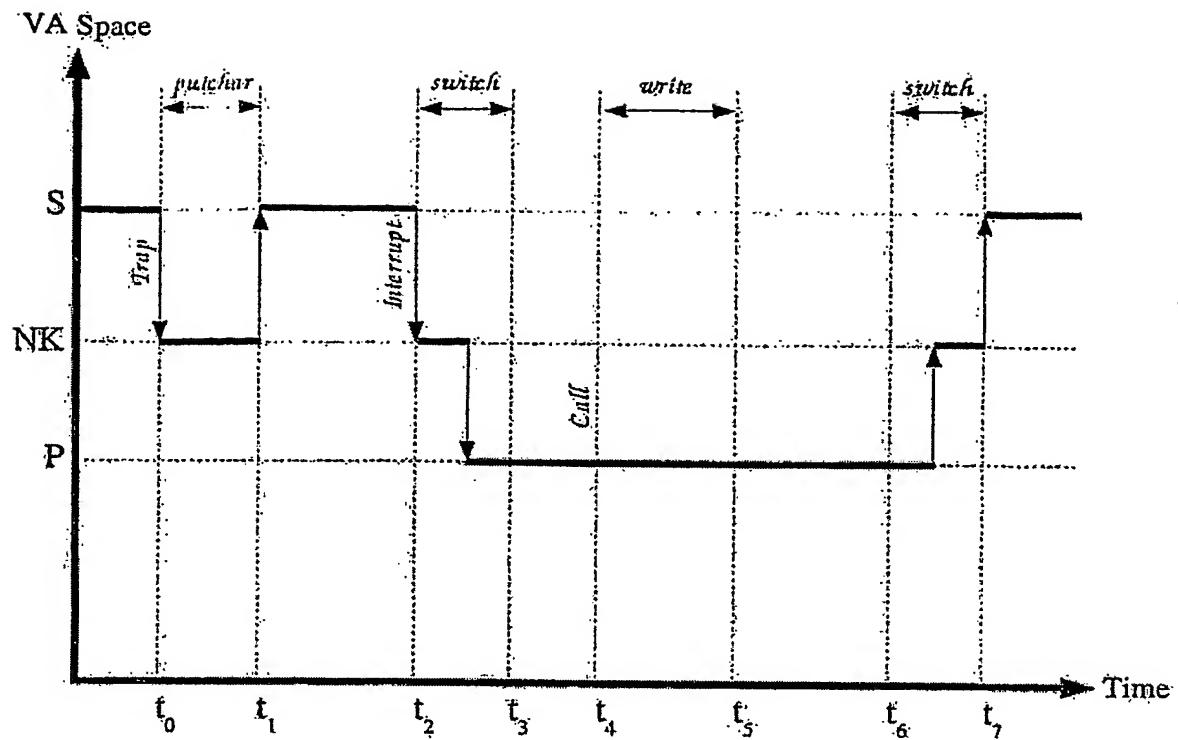


Fig. 11 Virtual Address Space Switching

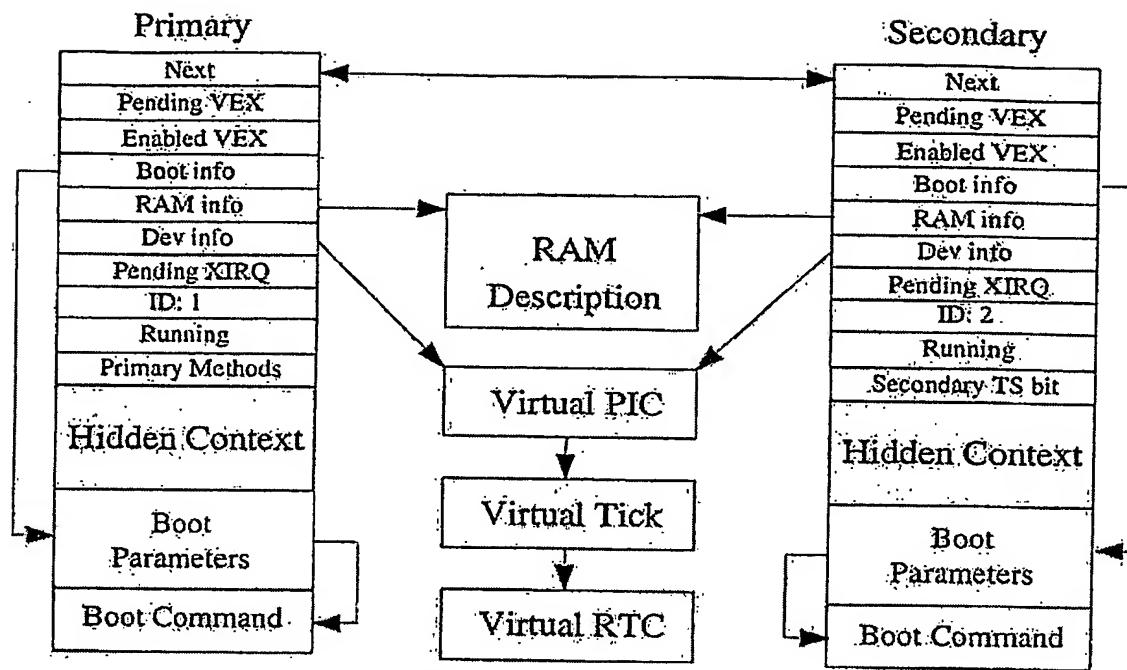


Fig. 12. Visible Kernel Context

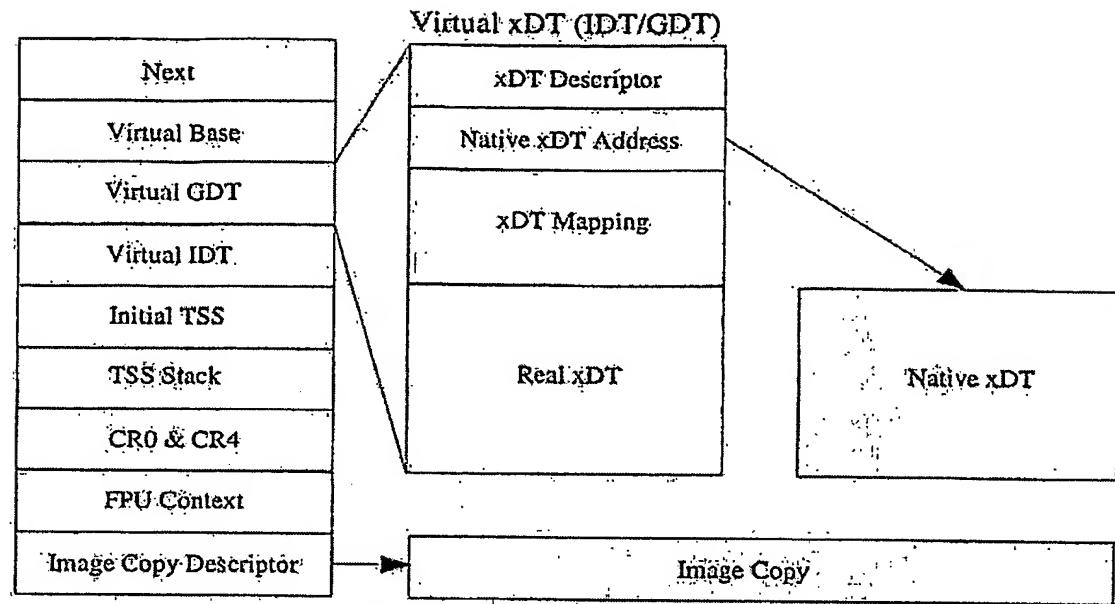


Fig. 13 Hidden Kernel Context

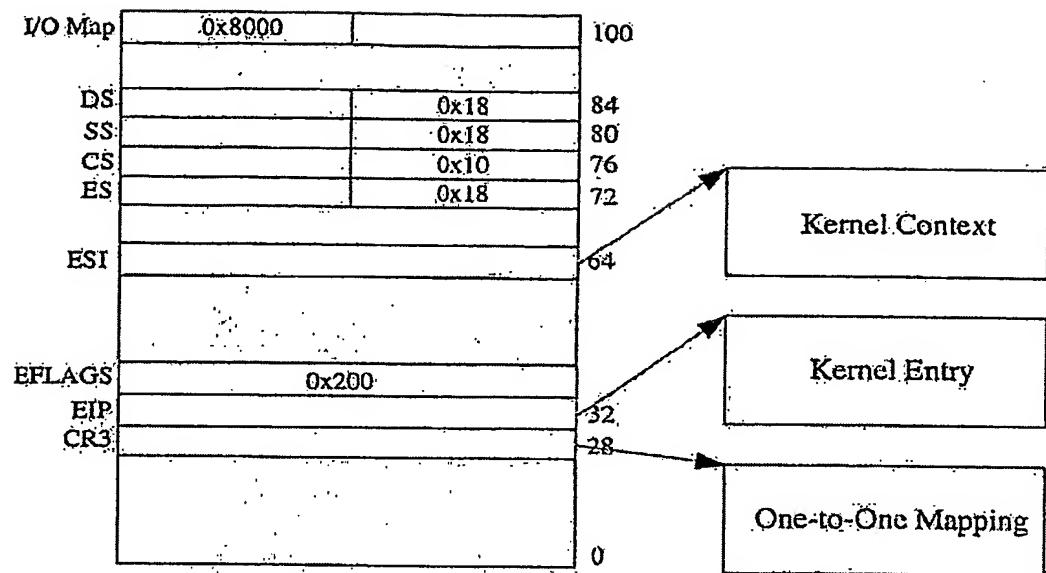


Fig. 14 Initial TSS

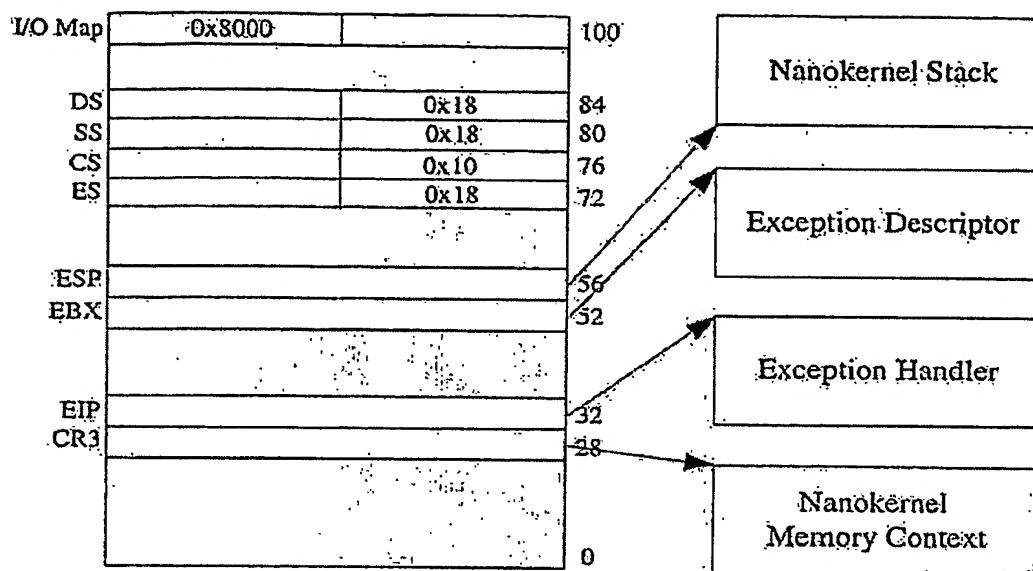


Fig. 15 Nanokernel TSS

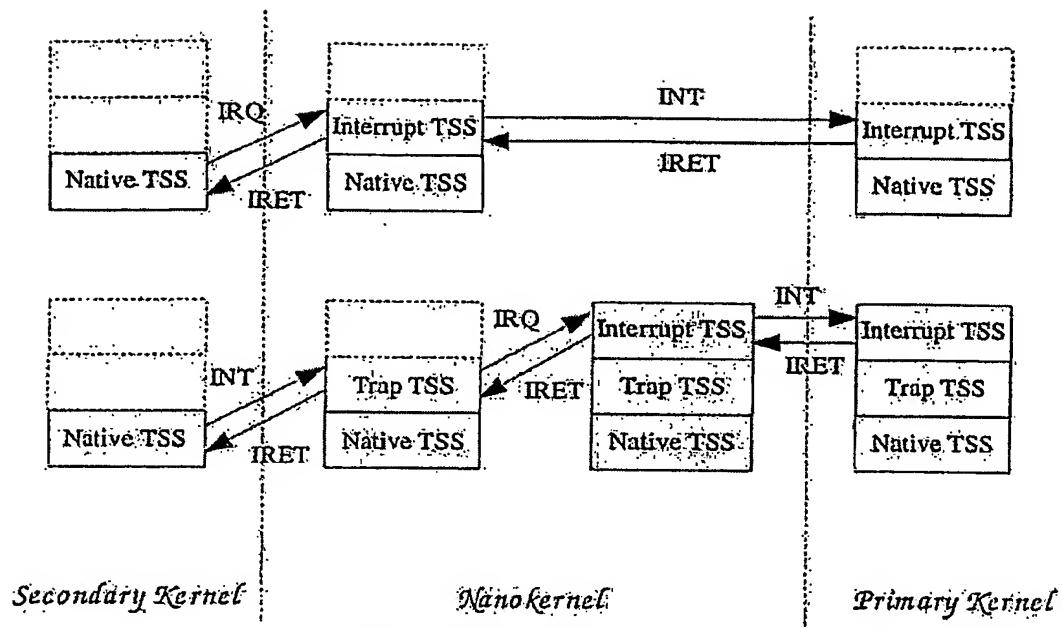


Fig. 16 Nanokernel TSS Stack

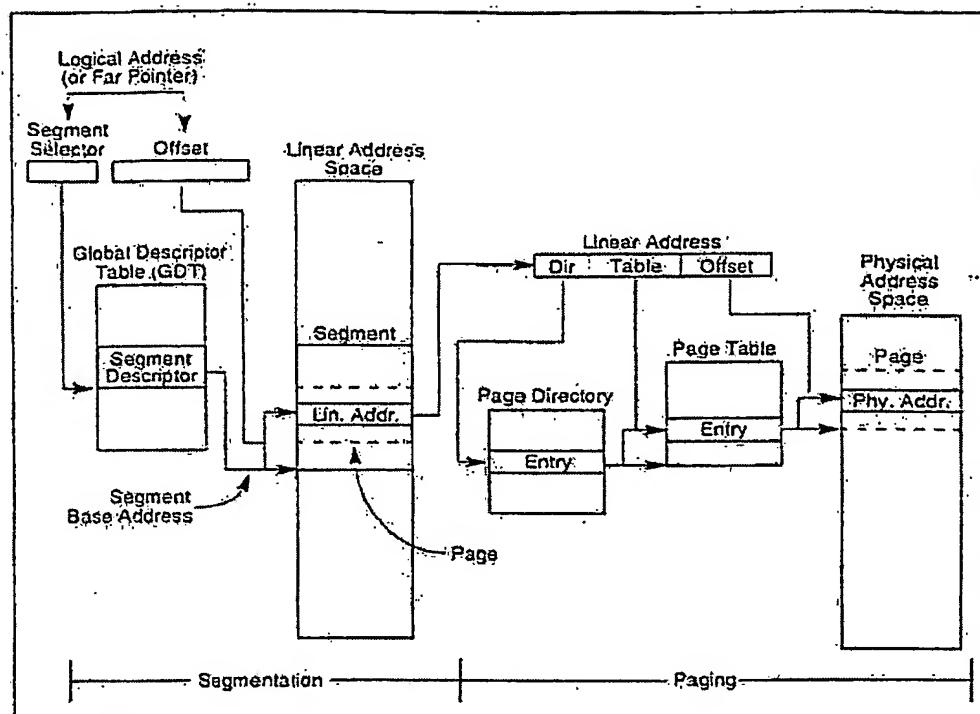


FIG. 17

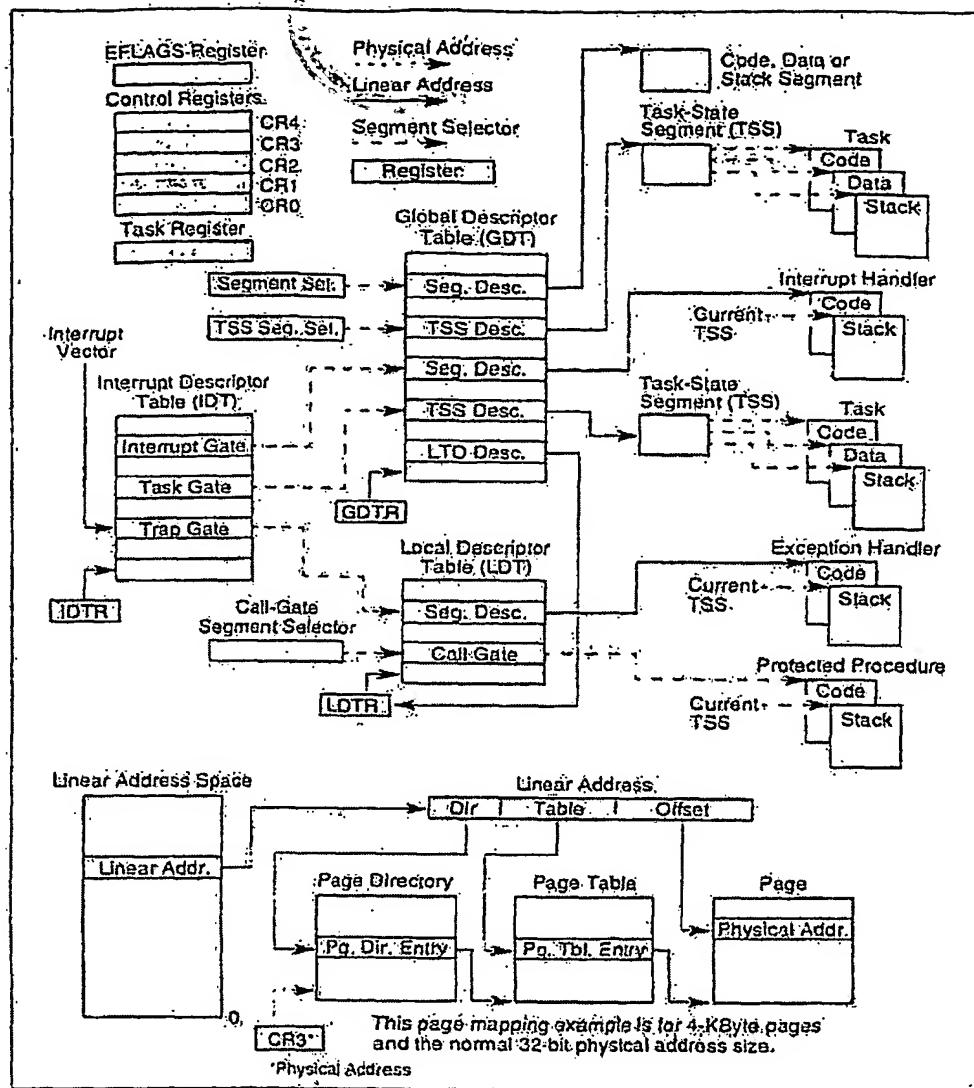


FIG. 18